Abstract of the Disclosure:

A semiconductor memory device is described that is formed of a semiconductor substrate. An insulating layer is disposed on the semiconductor substrate. A matrix of semiconductor memory elements is disposed in the substrate. The semiconductor memory elements include a plurality of contact holes formed in the insulating layer. One contact hole is formed in the insulating layer for each of the semiconductor memory elements. A bit definition region is disposed in the semiconductor substrate underneath each of the contact holes. A contact plug is disposed in each of the contact holes and is in electrical contact with the bit definition region. The bit definition region is configured such that a contact resistance between the semiconductor substrate and the contact plug defines a bit to be stored in the semiconductor memory elements. An evaluation circuit is connected to and evaluates the contact resistance of the semiconductor memory elements.

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